**WHAT IS CLAIMED IS:**

1. A computer-implemented method for handling data using a plurality of processors, the method comprising:

dividing a common memory, accessible to one or more first processors and to one or more secondary processors, into a plurality of data blocks using one of the first processors, the one or more first processors and the one or more second processors being chosen from a group of heterogeneous processors;

identifying an available processor from the secondary processors to process one of the data blocks; and

processing the data block using the available secondary processor.

2. The method of Claim 1, further comprising directly accessing the data block in the common memory using a memory access unit of the available secondary processor.

3. The method of Claim 2, further comprising transferring the data block using the available secondary processor from the common memory to a secondary memory local to the available secondary processor.

4. The method of Claim 3, further comprising transferring the data block using the available secondary processor from the secondary memory to the common memory after processing the data block.

5. The method of Claim 1, further comprising the available secondary processor notifying one of the first processors after processing the data block.

6. The method of Claim 1, further comprising requesting, using one of the first processors, the secondary processor to process the data block.

7. The method of Claim 1, wherein the dividing comprises dividing the common memory into data blocks, a size of the data blocks equaling a size of registers of the available secondary processor.

8. The method of Claim 1, further comprising processing the data block further using one of the first processors.

9. The method of Claim 1, further comprising identifying, using one of the first processors, additional available secondary processors to process data blocks until all the data blocks have been processed.

10. An information handling system comprising:

a plurality of heterogeneous processors, wherein the plurality of heterogeneous processors comprises one or more first processors and one or more secondary processors; and

a common memory accessible by the plurality of heterogeneous processors, wherein:

one of the first processors is adapted to divide the common memory into a plurality of data blocks,

one of the first processors is adapted to identify an available processor from the secondary processors to process one of the data block; and

one of the secondary processors is adapted to process the data block.

11. The information handling system of Claim 10, wherein the available secondary processor is further adapted to directly access the data block in the common memory using a memory access unit.

12. The information handling system of Claim 11, wherein the available secondary processor is further adapted to transfer the data block from the common memory to a secondary memory local to the available secondary processor.

13. The information handling system of Claim 12, wherein the available secondary processor is further adapted to transfer the data block from the secondary memory to the common memory after processing the data block.

14. The information handling system of Claim 10, wherein the available secondary processor is further adapted to notify one of the first processors after processing the data block.

15. The information handling system of Claim 10, wherein one of the first processors is adapted to request the available secondary processor to process the data block.

16. The information handling system of Claim 10, wherein the one first processor is further adapted to divide the common memory into data blocks, a size of the data blocks equaling a size of registers of one of the secondary processors.

17. The information handling system of Claim 10, wherein one of the first processors is adapted to further process the data block.

18. The information handling system of Claim 10, wherein one the first processors is adapted to identify additional available secondary processors to process data blocks until all the data blocks have been processed.

19. A computer program product on computer operable media, the computer program product comprising:

means for dividing a common memory, accessible to one or more first processors and to one or more secondary processors, into a plurality of data blocks, wherein the one or more first processors and the one or more second processors are selected from a group of heterogeneous processors;

means for identifying an available processor from the secondary processors to process one of the data blocks; and

means for processing the data block using the available secondary processor.

20. The computer product of Claim 19, further comprising means for directly accessing the data block in the common memory.

21. The computer product of Claim 20, further comprising means for transferring the data block from the common memory to a secondary memory local to the available secondary processor.

22. The computer product of Claim 21, further comprising means for transferring the data block from the secondary memory to the common memory after processing the data block.

23. The computer product of Claim 19, further comprising means for notifying one of the first processors after processing the data block.

24. The computer product of Claim 19, further comprising means for requesting the secondary processor to process the data block.

25. The computer product of Claim 19, wherein the means for dividing comprises means for dividing the common memory into data blocks, a size of the data blocks equaling a size of registers of the secondary processors.

26. The computer product of Claim 19, further comprising means for processing the data block further.

27. The computer product of Claim 19, further comprising means for identifying additional available secondary processors to process data blocks until all the data blocks have been processed.